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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,716	08/28/2001	Kazushige Yonenaga	011070	2708

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EXAMINER	
LEUNG, WAI LUN	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,716	YONENAGA ET AL.	
	Examiner	Art Unit	
	Danny Wai Lun Leung	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-16* is/are rejected.

7)☒ Claim(s) *13,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/28/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/29/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 8/30/2000. It is noted, however, that applicant has not filed a certified copy of the Japan 261114/2000 application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 8, 10-12, and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In page 21, line 22-26, paragraph 72, of the specification, applicant described "the length and/or shape of electrodes are not designed for high speed operation, but designed to satisfy desired bandwidth restriction performance by using loss in an electrode", but failed to describe in detail how loss of traveling wave type electrode restricts bandwidth as described in claim 8, which claims 10-12, and 16 are dependent upon.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,543,952 to Yonenaga et al., in reference to Chapter 7, Introduction to CMOS design, by E. Di Zitti, WP3 Electronic Engineering Pilot University of Genoa.

Regarding to claim 1, Yonenaga discloses an optical transmitter (fig 1b) comprising: an input terminal (col 3, ln 34) for accepting an electrical binary signal (col 3, ln 35), bandwidth restriction means (col 4, ln 14-16) for restricting bandwidth of said electrical binary signal, an electrical-optical conversion means (col 3, ln 37-45) for converting said electrical signal which is bandwidth restricted by said bandwidth restriction means to an optical signal. An amplifier (11, fig 1B; where an inverter is inherently an amplifier, as described in Chapter 7, Introduction to CMOS design, by E. Di Zitti, WP3 Electronic Engineering Pilot University of Genoa) for amplifying an input signal of said electrical-optical conversion means so that said input signal has enough level for operating said electrical-optical conversion means (col 5, ln 66-col 6, ln 3), wherein said bandwidth restriction means locates between an output of said amplifier and an input of said electrical-optical conversion means (75b, fig 1B).

Regarding to claim 2, Yonenaga discloses an optical transmitter wherein a precoding means (80, fig 1B) is provided at an input stage of said amplifier, said precoding means provides a binary output which is the same as the previous output when an input binary digital signal is 0,

and an output which differs from the previous output when an input digital signal is 1 (col 5, ln 59-65), and said bandwidth restriction means is a low- pass filter which generates a ternary duobinary signal (75b, fig 1B; col 6, ln 50-54).

Regarding to claim 3, Yonenaga discloses an optical transmitter wherein said electrical-optical conversion means provides the maximum level of optical output for an input electrical signal having the maximum level and the minimum level (col 9, ln 23-32), the minimum level of optical output for an input electrical signal having middle level between said maximum level and said minimum level (col 9, ln 23-32), and optical phase of said maximum level of said optical signal is opposite of optical phase of said minimum level of said optical signal (col 9, ln 29).

Regarding to claim 4, Yonenaga discloses an optical transmitter wherein said electrical-optical conversion means is a Mach Zehnder light intensity modulator having a pair of electrodes which are driven by ternary electrical duobinary signals having opposite polarities (col 8, ln 32-39).

Regarding to claim 5, Yonenaga discloses an optical transmitter wherein at least two of said bandwidth restriction means, said electrical-optical conversion means, and said amplifier are integrated in a single module (fig 1B, where everything is in one module).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-7, 9, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,543,952 to Yonenaga et al, in view of US Patent Number 5,644,664 to Burns et al., in reference to Chapter 7, Introduction to CMOS design, by E. Di Zitti, WP3 Electronic Engineering Pilot University of Genoa.

Regarding to claim 6, Yonenaga discloses an optical transmitter in accordance to claim 5 contains electrical-optical conversion means, but does not disclose expressly that the electrical-optical conversion means has function as bandwidth restriction means. Burns, from the same field of endeavor, discloses an optical transmitter contains electrical-optical conversion means that has function as the bandwidth restriction means (col 9, ln 38-39). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate Burns' electrical-optical conversion means that has function as bandwidth restriction means with Yonenaga's optical transmitter in order to restrict bandwidth by using the electrical-optical conversion means without additional filtering components in the system such that the size and cost of the transmitter could be lowered.

Regarding to claim 7, Yonenaga discloses an optical transmitter (fig 1B) comprising: an input terminal (col 3, ln 34) for accepting an electrical binary signal (col 3, ln 35), an electrical-optical conversion means (col 3, ln 37-45) for converting an electrical signal to an optical signal, an amplifier (11, fig 1B; where an inverter is inherently an amplifier, as described in Chapter 7, Introduction to CMOS design, by E. Di Zitti, WP3 Electronic Engineering Pilot University of Genoa) for amplifying an input signal applied to the input terminal to level requested for operating an electrical-optical conversion means, and applying the amplified electrical signal to the electrical-optical conversion means (75b, fig 1B). Yonenaga does not disclose expressly that

the electrical-optical conversion means have a traveling wave type electrode operating to restrict bandwidth of an output light of the electrical-optical conversion means. Burns, from the same field of endeavor, discloses an electrical-optical conversion means having a traveling wave type electrode operating to restrict bandwidth of an output light of an electrical-optical conversion means (col 4, ln 16-33). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate Burns' electrical-optical conversion means with Yonenaga's optical transmitter in order to restrict bandwidth by using the electrical-optical conversion means without additional filtering components in the system such that the size and cost of the transmitter could be lowered.

Regarding to claim 9, the combination of Yonenaga and Burns teaches an optical transmitter according to claim 6 or claim 7 as discussed above. Yonenaga further teaches that the electrical-optical conversion means is a Mach Zehnder light intensity modulator (col 8, ln 31-39) having a traveling wave type electrode. Burns further teaches that the bandwidth of optical output of the mach Zehnder light intensity modulator is restricted by using mismatching of phase velocity of electric wave (col 9, ln 38-39) propagating the traveling wave type electrode and optical wave propagating in an optical waveguide having refractive index depending upon electrical field generated by the electric wave (col 12, ln 16-27).

Regarding to claim 14, Burns further teaches an optical transmitter in accordance to claim 9, wherein said Mach Zehnder Light intensity modulator is provided on a substrate of Z-cut Lithium-Niobate (col 11, ln 7).

Regarding to claim 15, Burns further teaches an optical transmitter in accordance to claim 9, wherein said Mach Zehnder light intensity modulator is provided on a substrate of X-cut Lithium-Niobate (col 11, ln 7).

Allowable Subject Matter

7. Claims 13, 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Wai Lun Leung whose telephone number is (571)272-5504. The examiner can normally be reached on 9am-5pm Mon-Fri, except federal holidays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

19 July 2005

JASON CHAN
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